Performance Improvement In Packet Buffers For High Bandwidth Routers

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INTRODUCTION

• Internet routers play a crucial role in sustaining growth of internet by being able to switch packets extremely fast to keep up with the growing bandwidth.

• Packet buffers need to be designed to support large capacity, multiple queues, and provide short response times.

• This method we present scalable, efficient, and novel distributed packet buffer architecture.
In order to support fine-grained IP quality of service (QoS) requirements, nowadays, a packet buffer usually maintains thousands of queues.

A packet buffer should be capable of sustaining continuous data streams for both ingress and egress, with the ever-increasing line rate, memory.

We first propose a memory management algorithm (MMA) called Random Round Robin (RRR). Thereafter, we devise a “traffic-aware” approach which aims to provide different services for different types of data streams.
Problems in the Existing System:

- Large size SRAM and high time complexity in memory management.
- The size of buffers in backbone routers was very small at the expense of a small loss in throughput.
- The router buffer sizing is still a big issue.
Proposed System

- We devise a “traffic-aware” approach which aims to provide different services for different types of data streams.

- This approach reduces the system overhead.

- The Mathematical analysis and Simulation together with its algorithm reduce the overall SRAM requirement significantly.

- This System provides guaranteed performance in terms of low time complexity, upper bounded drop rate, and uniform allocation of resources.
System Requirements

Hardware Requirements

- Processor: Intel I3
- Ram: 2GB.
- Hard Disk: 80 GB.
- Compact Disk: 650 MB.
- Input device: Standard Keyboard and Mouse.
- Output device: VGA and High Resolution Monitor.

Software Requirements

- Language: Java
Modules

- DISTRIBUTED PACKET BUFFER ARCHITECTURE
- COMPACT PACKET BUFFER DESIGNING
- DISTRIBUTED MEMORY HIERARCHY
DISTRIBUTED PACKET BUFFER ARCHITECTURE

- The overall packet buffer takes the form of a distributed system composed of several compact packet buffers.

- The packet buffer should be able to absorb incoming traffic at a given rate, and maintain the outgoing traffic at the same rate, while still supporting the requirements for the different data streams transiting through the buffer.
Performance improvement with different configurations:

(a) Theoretical value, $b=1\text{cell}$
(b) Practical measured value, $b=1\text{cell}$
(c) Practical measured value, $b=2\text{cells}$

(b) $b=2\text{cells}$, 30% Traffic Intensity
- Measured at tail cache
- Measured at front-buffer

Statistical interval = 10 timeslots
A new memory architecture that reduces the system overhead in term of SRAM size while relying on a nonspecific traffic pattern.

The required size of SRAM in the egress can be also reduced significantly by using RRR-MMA with an extra arbiter.
A distributed packet buffer system consisting of three compact packet buffers. Queues are mapped to the compact packet buffers and this information is tracked in the queue table.
The packet distributor implements a suitable load-balancing scheme that keeps track of the information of each compact buffer, including the utilization of storage and bandwidth, and the number of active physical queues.
Use case Diagram:
Class Diagram:

```
source
+ip
+txt
+dest ip()
+send()

router
+source ip
+dest ip
+send()

Destination
+ip
+txt
+receive()
```
Sequence Diagram:

1: give destination ip address()
2: select message()
3: send ip address()
4: send data()
State machine Diagram:

- Source
- Router
- Destination
SCREEN SHOTS

Source Router:
Ingress Router:
Details about Routers:
source:
nullSource: localhost
Message: hi this is the message from source
Destination:

Click OK
1 Packet(s) Received

OK
Message:

Packet 1: hi this is the message from someone
Monitoring packets:
CONCLUSION

- Building packet buffers based on a hybrid SRAM/DRAM architecture while introducing minimum overhead is the major issue discussed in this paper.

- Exploring the advantage of parallel DRAMs leading to the requirement of small size SRAM and low time complexity in memory management.
THANK U